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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,579	10/23/2003	Noriyuki Miura	MAE 296	5973

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EXAMINER	
MOVVA, AMAR	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
04/10/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/690,579	MIURA, NORIYUKI	
	Examiner	Art Unit	
	AMAR MOVVA	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-6,8,9,11-14 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,8,9,11-14 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1,3-6,8-9,11-14, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nathanson '385 in view of Yamazaki '185/Dennen '869/Kao '700.

a. Regarding claims 1,3-6, and 8:

i. Nathanson discloses a semiconductor device comprising: a semiconductor substrate (43, fig. 3); an insulating layer (45, fig. 3) disposed on said semiconductor substrate; an SOl film (51,47,49, fig. 3) disposed on said insulating layer; a gate insulator (53, fig. 3) disposed on said SOl film; and a gate electrode (55, fig. 3) disposed on said gate insulator; wherein a source (47, fig. 3), a drain (49, fig. 3), and a channel (51, fig. 3)are formed in said SOl film so that said gate insulator is located at least between said channel and said gate electrode, thereby forming a MOSFET including said source, said drain, said channel, said gate electrode, and said gate insulator (fig. 3); and wherein said gate electrode is made of polysilicon and conductivity types of said source, said drain, and said channel are all N-type (fig. 3), a channel length of said channel is within a range of approximately from 0.1 um to 0.25 um (col. 5). A thickness of said gate insulator is approximately 2 nm (col., and said thickness of said SOl film is approximately

20 nm (col. 3). Said channel length of said channel is approximately 0.15 um (col. 5). Nathanson, however, does not expressly disclose that the channel has an impurity concentration of approximately 3x10^17/ cm^3, the, source and drain have an impurity concentration not less than approximately 1X10^21/cm^3, and the gate electrode to be doped p-type.

ii. Yamazki discloses MOSFET wherein the first and second n-channel transistors wherein the area under the source and drain have an impurity concentration of 1x10^20 to 1x10^21/cm^3 ([Embodiment 1],fig. 2a-5b). Kao discloses a n-channel/n-source/n-drain MOSFET wherein the channel impurity concentration is approximately 3x10^17/cm^3 (lines 25-35, col. 4). Dennen discloses a a n-channel/n-source/n-drain MOSFET wherein the gate electrode is p-type polysilicon (lines 50-55, col. 8)

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Yamazaki's/Kao's higher impurity concentrations in Nathanson's device since it would allow for better conductivity/device speed and allow for variable threshold voltage FETs. Additionally It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Dennen's p-type gate electrode in Nathanson's device since it would allow for a functional NNN type low power device (Nathanson does not state what conductivity type the gate poly-Si is.)

b. Regarding claims 9,11-14, and 16:

i. Nathanson discloses a metal-oxide-semiconductor field-effect transistor comprising: a semiconductor substrate having a substrate (43, fig. 3), an insulating layer (45, fig. 3) which is disposed on the substrate and a silicon layer (51,47,49, fig. 3) which is disposed on the insulating layer; a gate insulator (53, fig. 3) disposed on the silicon layer of the semiconductor substrate; a gate electrode (55, fig. 3), which is made of P-type polysilicon, disposed on the semiconductor substrate so that the gate insulator is disposed between the gate electrode and the semiconductor substrate (fig. 3); a channel region (51, fig. 3) formed in the silicon layer, which is located under the gate electrode; and a source (47, fig. 3) and a drain (49, fig. 3) formed in the silicon layer and being adjacent to the channel region; wherein conductivity types of the channel region, the source and the drain are all N-type (fig. 3), a channel length of the channel region is within a range approximately from 0.1 um to 0.25 um (col. 5). Nathanson, however, does not expressly disclose that the channel has an impurity concentration of approximately 3x10^17/ cm^3, the, source and drain have an impurity concentration not less than approximately 1X10^21/cm^3, and the gate electrode to be doped p-type.

ii. Yamazki discloses MOSFET wherein the first and second n-channel transistors wherein the area under the source and drain have an impurity concentration of 1x10^20 to 1x10^21/cm^3 ([Embodiment 1],fig. 2a-5b). Kao discloses a n-channel/n-source/n-drain MOSFET wherein the channel impurity concentration is approximately 3x10^17/cm^3 (lines 25-35, col. 4). Dennen

discloses a a n-channel/n-source/n-drain MOSFET wherein the gate electrode is p-type polysilicon (lines 50-55, col. 8)

iii. It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Yamazaki's/Kao's higher impurity concentrations in Nathanson's device since it would allow for better conductivity/device speed and allow for variable threshold voltage FETs. Additionally It would have been obvious to one of ordinary skill in the art at the time of the invention to have used Dennen's p-type gate electrode in Nathanson's device since it would allow for a functional NNN type low power device (Nathanson does not state what conductivity type the gate poly-Si is.)

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amar Movva whose telephone number is 571-272-9009. The examiner can normally be reached on 7:30 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Amar Movva
Examiner
Art Unit 2891

am

/BRADLEY W BAUMEISTER/

Supervisory Patent Examiner, Art Unit 2891